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jv809 U.S. PTO 04/17/00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No. SE1443PDA50021A

Anticipated Classification of this application: Class___

Prior Application:
Examiner: A. Wilson
Art Unit: 2815

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jc511 U.S. PTO 09/551187 04/17/00

BOX DIVISIONAL
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir: This is a request for filing a

[ ] Continuation

application under 37 CFR 1.53(b)

[X] Divisional

of pending prior application Serial No. 09/107,721 filed on June 30, 1998 of Jun ZENG
(date) (inventor currently of record in prior application)

for **SEMICONDUCTOR DEVICE HAVING REDUCED EFFECTIVE SUBSTRATE RESISTIVITY AND ASSOCIATED METHODS**
(title of invention)

1. [X] Enclosed is a copy of the prior application, including the oath or declaration as originally filed and an affidavit or declaration verifying it as a true copy.

2. [ ] Prepare a copy of the prior application.

3 [X] A preliminary amendment is enclosed. (Claims added by this amendment have been properly numbered consecutively beginning with the number next following the highest numbered original claim in the prior application.)

4. [X] The filing fee is calculated below:

Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
Attorneys At Law, 255 South Orange Avenue, Suite 1401, P.O. Box 3791, Orlando, Florida 32802-3791

CLAIMS AS FILED IN THE PRIOR APPLICATION, LESS ANY CLAIMS CANCELED BY AMENDMENT BELOW:

	(Col. 1)		(Col. 2)		SMALL ENTITY			LARGE ENTITY	
FOR:	# FILED		# EXTRA		RATE	FEE		RATE	FEE
BASIC FEE						$ 380	OR		$ 760
TOTAL CLAIMS	24	-20	4		X 9	$	OR	X 18	$ 72
INDEP CLAIMS	2	- 3	- -		X 39	$	OR	X 78	$ - -
[ ] MULTIPLE DEPENDENT CLAIM PRESENTED						$	OR		
* If the difference in Col. 1 is less than "0", enter "0" in Col. 2.					TOTAL	$		TOTAL	$ 832

5. [X] A check in the amount of $832.00 is enclosed. If any additional extension and/or fee is required, or if any additional fee for claims is required, charge Account No. 01-0484.

6. [X] Cancel in this application original claims 1-51 of the prior application before calculating the filing fee.

7. [X] Amend the specification by inserting before the first line the sentence:
--This application is a division of Serial No. 09/107,721 filed on June 30, 1998 , the disclosures of which are hereby incorporated by reference in their entirety.--

8. [ ] Transfer the drawings from the prior application to this application and abandon said prior application as of the filing date accorded this application. A duplicate copy of this sheet is enclosed for filing in the prior application file. (May only be used if signed by person authorized by Rule 138 and before payment of base issue fee.)

9a. [X] New formal drawings are enclosed.

9b. [ ] Priority of application Serial No. _____ filed on _____ in _____ (country) is claimed under 35 U.S.C. 119.

9c. [ ] The certified copy has been filed in prior application Serial No. _____ filed _____.

10. [X] The prior application is assigned of record to **Intersil Corporation**.

11. [X] Citation Under 37 CFR 1.97 and PTO-1449.

Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
Attorneys At Law, 255 South Orange Avenue, Suite 1401, P.O. Box 3791, Orlando, Florida 32802-3791

12. [X] The power of attorney in the prior application is to: Christopher F. Regan, No. 34,906; **Herbert L. Allen**, Reg. No. 25,322; **David L. Sigalow,** Reg. No. 36,006; **Jeffrey S. Whittle,** Reg. No. 36,382; **Richard K. Warther,** Reg. No. 32,180; **Michael W. Taylor,** Reg. No. 43,182; **Henry Estevez**, Reg. No. 37,823; **Carl M. Napolitano,** Reg. No. 37,405; **Jacqueline E. Hartt,** Reg. No. 37,845; **Leslie J. Hart,** Reg. No. 26,462; **Harry M. Fleck,** Reg. No. 24,704; **John L. DeAngelis,** Reg. No. 30,622; **Ferdinand Romano,** Reg. No. 32,752; **Joel I. Rosenblatt,** Reg. No. 26,025; **Daniel J. Staudt,** 34,733; **Frederick R. Jorgenson,** 38,196; **Dennis L. Cook,** Reg. No. 30,826; and **Bidyut K. Niyogi,** Reg. No. 27,071 all of Allen, Dyer Doppelt Milbrath & Gilchrist, P.A. 255 S. Orange Avenue, Suite 1401, P.O. Box 3791, Orlando, Florida 32802-3791 (name, registration number and address)

a. [X] The power appears in the original papers in the prior application.

b. [ ] Since the power does not appear in the original papers, a copy of the power in the prior application is enclosed.

c. [X] Continue to address all future communications to:
Christopher F. Regan, No. 34,906; (fill in)
Allen, Dyer Doppelt Milbrath & Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401, P.O. Box 3791, Orlando, Florida 32802-3791

13. [ ] Small entity status of this application under 37 CFR 1.19 and 1.27 has been established by a verified statement previously submitted.

14. [X] I hereby verify that the attached papers are a true copy of prior application Serial No. 09/107,721 as originally filed on June 30, 1998.

The undersigned declare(s) further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

April 17, 2000
Date

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[X] Attorney or agent of record
[ ] Inventor(s)
[ ] Assignee of complete interest
[ ] Filed under Rule 34(a)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
ZENG

Serial No. **Not yet assigned**

Filing Date: **Herewith**

For: **SEMICONDUCTOR DEVICE HAVING REDUCED EFFECTIVE SUBSTRATE RESISTIVITY AND ASSOCIATED METHODS**

Examiner: A. Wilson

Art Unit: 2815

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

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Eric Liles

(TYPED OR PRINTED NAME OF PERSON MAILING PAPER OR FEE)

Eric Liles

(SIGNATURE OF PERSON MAILING PAPER OR FEE)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Claims:

Please cancel Claims 1-51

Please add new Claims 52-75.

52. A method for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method comprising:

forming at least one device active region in the semiconductor substrate adjacent a first surface thereof;

forming at least one recess extending from a second surface of the substrate, opposite the first surface, into interior portions of the semiconductor substrate; and

forming at least one resistivity-lowering body in the least one recess of the semiconductor substrate, the at least one resistivity-lowering body comprising a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate.

53. A method according to Claim 52 further comprising forming an electrical contact layer on the second surface of the semiconductor substrate being electrically connected to the at least one resistivity-lowering body.

54. A method according to Claim 52 wherein forming the at least one resistivity-lowering body comprises filling an associated recess.

55. A method according to Claim 52 further comprising forming a barrier layer lining the at least one recess.

56. A method according to Claim 52 wherein forming the at least one resistivity-lowering body comprises forming same using an electrical conductor having an electrical resistivity less than about 10^{-4} Ω•cm.

57. A method according to Claim 52 wherein forming the at least one recess and associated resistivity-lowering

body comprises forming same to define a proportion of the semiconductor substrate area adjacent the at least one device active region greater than about 0.4 percent.

58. A method according to Claim 52 wherein forming the at least one recess and associated resistivity-lowering body comprises forming same to extend into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

59. A method according to Claim 52 wherein forming the at least one recess and associated resistivity-lowering body comprises forming an array of recesses and associated resistivity-lowering bodies.

60. A method according to Claim 59 wherein forming the array of recesses and associated resistivity-lowering bodies comprises forming same to be arranged in a grid pattern.

61. A method according to Claim 60 wherein forming the grid pattern comprises cutting trenches in the second surface of the semiconductor substrate.

62. A method according to Claim 52 wherein forming the at least one device active region comprises forming at least one device active region for a metal-oxide semiconductor field-effect transistor (MOSFET).

63. A method according to Claim 52 wherein forming the at least one device active region comprises forming at least one device active region for an insulated gate bipolar transistor (IGBT).

64. A method according to Claim 52 wherein forming the at least one device active region comprises forming at least one active region of a microprocessor.

65. A method for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method comprising:

forming at least one device active region in the semiconductor substrate adjacent a first surface thereof; and

forming at least one resistivity-lowering body extending from a second surface of the substrate, opposite the first surface, into interior portions of the semiconductor substrate, the at least one resistivity-lowering body comprising a material different than the semiconductor substrate and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate

66. A method according to Claim 65 further comprising forming an electrical contact layer on the second surface of the semiconductor substrate being electrically connected to the at least one resistivity-lowering body.

67. A method according to Claim 65 wherein forming the at least one resistivity-lowering body comprises forming

same using an electrical conductor having an electrical resistivity less than about 10^{-4} Ω•cm.

68. A method according to Claim 65 wherein forming the at least one resistivity-lowering body comprises forming same to define a proportion of the semiconductor substrate area adjacent the at least one device active region greater than about 0.4 percent.

69. A method according to Claim 65 wherein forming the at least one resistivity-lowering body comprises forming same to extend into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

70. A method according to Claim 65 wherein forming the at least one resistivity-lowering body comprises forming an array of resistivity-lowering bodies.

71. A method according to Claim 70 wherein forming the array of resistivity-lowering bodies comprises forming same to be arranged in a grid pattern.

72. A method according to Claim 71 wherein forming the grid pattern comprises cutting trenches in the second surface of the semiconductor substrate.

73. A method according to Claim 65 wherein forming the at least one device active region comprises forming at

least one device active region for a metal-oxide semiconductor field-effect transistor (MOSFET).

74. A method according to Claim 65 wherein forming the at least one device active region comprises forming at least one device active region for an insulated gate bipolar transistor (IGBT).

75. A method according to Claim 65 wherein forming the at least one device active region comprises forming at least one active region of a microprocessor.

REMARKS

It is believed that all of the claims are patentable over the prior art. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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SEMICONDUCTOR DEVICE HAVING REDUCED EFFECTIVE SUBSTRATE RESISTIVITY AND ASSOCIATED METHODS

Field of the Invention

The present invention relates to semiconductors, and, more particularly, to a semiconductor device, such as a power MOSFET having reduced on-resistance.

Background of the Invention

Semiconductor devices, typically in the form of integrated circuits, are widely used in almost all electronic equipment, such as handheld calculators, personal computers, automobiles, cellular telephones, and sophisticated mainframe computers. A typical semiconductor device includes a semiconductor substrate which, in turn, includes a number of active devices formed adjacent a first surface of the substrate. For example, one or more power metal-oxide semiconductor field-effect transistors (MOSFETs) may be formed in active regions of the substrate. Power MOSFETs are often used because of their relatively high switching speeds as compared to bipolar transistors, for example. Power MOSFETs may be used in power conversion or motor control circuitry.

The so-called "on-resistance" of a power MOSFET

affects its power handling capability, as well as its operating energy efficiency. A higher on-resistance translates into greater power dissipation required for the chip. In addition, for portable battery-powered devices, for example, higher energy efficiency may be a primary concern to thereby extend battery life. In other words, in many applications it may be desired to provide low-voltage MOSFETs with a lower on-resistance.

To address this goal, the power semiconductor industry has been adopting very large scale integration (VLSI) technologies to increase device cell densities. For example, U.S. Patent No. 5,635,742 to Hoshi et al. discloses a lateral double-diffused MOSFET wherein source and drain openings are cyclically arranged so that at least two rows of source openings are arranged between adjacent drain openings to thereby reduce the on-resistance. Such common approaches to reducing the on-resistance have concentrated on reducing the contribution to the on-resistance of the scalable components of the integrated circuit, such as channel resistance.

Unfortunately, the on-resistance contribution from the unscalable regions of the integrated circuit, such as the substrate, for example, remain constant even as cell densities are increased. Moreover, as the cell densities increase further, the substrate on-resistance becomes almost a dominating factor for lower-voltage power MOSFETs which typically operate at less than about 30 V. For example, a 14 mil thick, N-type substrate with a resistivity of 4.5 $m\Omega \cdot cm$ has a specific on-resistance of 0.16 $m\Omega \cdot cm^2$. The relatively high resistivity of conventional substrates may also cause undesired contact resistance with a backside

contact layer, for example.

Currently, the die specific on-resistance of a 30 V MOSFET as offered by Fairchild under the designation FDS 6680, for example, has a specific on-resistance of 0.279 $m\Omega \cdot cm^2$. This demonstrates that if the 14 mil substrate was used, more than half of the device specific on-resistance would come from the substrate. Accordingly, one of the most significant efforts for producing the next generation of power MOSFETs will be to reduce the specific on-resistance of the substrate.

Since the substrate specific on-resistance is the product of its thickness and resistivity, there are two ways to reduce the specific on-resistance. The first is simply to thin the wafer from which the device is made. The second approach is to lower the substrate resistivity. Unfortunately, thinning the wafer is complicated and relatively expensive. In addition, too thin of a substrate may be difficult to handle and the production yield may be too low. Relating to lowering the resistivity of the substrate, the resistivity is currently limited by the silicon or other semiconductor material properties.

Summary of the Invention

In view of the foregoing background, it is therefore an object of the present invention to provide a semiconductor device and associated manufacturing method for reducing the effective substrate resistivity, such as to reduce specific on-resistance for power MOSFETs, for example.

This and other objects, features, and advantages in accordance with the present invention are provide by a semiconductor device comprising at least one device active region formed in a first

surface of a semiconductor substrate, an electrical contact layer on a second surface of the semiconductor substrate, and at least one resistivity-lowering body positioned in a corresponding recess in the substrate and connected to the electrical contact layer. The at least one resistivity-lowering body preferably comprises a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate to thereby lower an effective electrical resistivity of the substrate.

In one embodiment, the resistivity-lowering body preferably fills an associated recess. In addition, the device active region may be an active region of a power control device, such as a MOSFET or IGBT, for example. The at least one device active region may be provided by a plurality of power control device cells, for example. The lowered effective resistivity of the substrate is particularly advantageous for a discrete power MOSFET having a breakdown voltage of less than about 50 V, and, more preferably less than about 30 V.

The resistivity-lowering body may preferably be an electrical conductor having a resistivity less than about 10^{-4} Ω•cm. For example, the material may be a metal, such as copper, aluminum, silver or solder. A barrier metal layer, such as titanium, may be provided between the resistivity-lowering body metal and the substrate.

In addition, the resistivity-lowering body may comprise polysilicon. The polysilicon may have its resistivity reduced by doping.

To reduce the contact resistance, a more highly doped layer may be formed in the substrate adjacent the resistivity-lowering bodies. A lower

resistivity substrate on the order of 3 mΩ•cm, for example, may also be used to lower the contact resistance.

The at least one recess and associated resistivity-lowering body preferably defines a proportion of the semiconductor substrate area adjacent the device active region greater than about 0.4 percent. The at least one recess and associated resistivity-lowering body preferably extends into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

In one particularly readily manufactured version of the semiconductor device, the at least one recess and associated resistivity-lowering body comprise an array of recesses and associated resistivity-lowering bodies. The recesses may be formed by sawing, cutting and/or etching a grid of intersecting trenches in the second surface of the substrate. Alternately, a plurality of individual spaced apart recesses and associated bodies may be provided.

The semiconductor substrate may comprise silicon, for example. In addition, since a metal, such as copper or aluminum may be used for the resistivity-lowering bodies, the thermal resistivity of these materials is typically lower than silicon, for example. Accordingly, power dissipation from the substrate is also enhanced.

A method aspect of the invention is for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity. The method preferably comprises the steps of: forming at least one device active region in the semiconductor substrate adjacent a first surface thereof; forming at least

one recess extending from a second surface of the substrate, opposite the first surface, into interior portions of the semiconductor substrate; and forming at least one resistivity-lowering body in the least one recess of the semiconductor substrate. The at least one resistivity-lowering body preferably comprises a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate. The method also preferably includes the step of forming an electrical contact layer on the second surface of the semiconductor substrate being electrically connected to the at least one resistivity-lowering body.

Brief Description of the Drawings

FIG. 1 is a schematic cross-sectional view of a semiconductor device in accordance with the present invention.

FIG. 2 is an enlarged schematic bottom plan view of an embodiment of the semiconductor device in accordance with the present invention with the contact layer removed to illustrate a grid pattern of recesses for resistivity-lowering bodies in the substrate.

FIG. 3 is a schematic cross-sectional view of another embodiment of the semiconductor device in accordance with the present invention.

FIG. 4 is an enlarged schematic bottom plan view of another embodiment of the semiconductor device in accordance with the present invention with the contact layer removed to illustrate an array of spaced apart recesses for the resistivity-lowering bodies in the substrate.

FIG. 5 is a schematic cross-sectional view of a portion of a power MOSFET semiconductor device in

accordance with the invention.

FIG. 6 is a schematic cross-sectional view of a portion of a power IGBT semiconductor device in accordance with the invention.

FIG. 7 is a graph of specific on-resistances versus percentage of body area to die area for a first set of examples.

FIG. 8 is a graph of specific thermal resistances versus percentage of body area to die area for the first set of examples.

FIG. 9 is a graph of specific on-resistances versus percentage of body area to die area for a second set of examples.

FIG. 10 is a graph of specific thermal resistances versus percentage of body area to die area for the second set of examples.

FIG. 11 is a graph of specific on-resistances versus percentage of body area to die area for a third set of examples.

FIG. 12 is a graph of specific thermal resistances versus percentage of body area to die area for the third set of examples.

FIG. 13 is a graph of specific on-resistances versus percentage of body area to die area for a fourth set of examples.

FIG. 14 is a graph of specific on-resistances versus percentage of body area to die area for a fifth set of examples.

Detailed Description of the Preferred Embodiments

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as

limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout, and the thicknesses of certain layers may be exaggerated in the drawings for clarity.

Referring initially to FIGS. 1 and 2 an embodiment of a semiconductor device **20** having a lowered effective substrate resistivity is described. The lowered effective substrate resistivity results in a lowered specific on-resistance, for example, when the invention is implemented in a power MOSFET device, for example, as will be readily appreciated by those skilled in the art. The semiconductor device **20** illustratively includes a plurality of device active regions **22** formed in a first or upper surface of a semiconductor substrate **23**. An electrical contact layer **25** is provided on a second surface or backside of the semiconductor substrate **23**. Moreover, a plurality of resistivity-lowering bodies **26** are positioned in corresponding recesses in the substrate **23** and are connected to the electrical contact layer **25**. The resistivity-lowering bodies **26** each preferably comprises a material having an electrical resistivity lower than an electrical resistivity of the material of the semiconductor substrate **23** to thereby lower an effective electrical resistivity of the substrate. The term "effective electrical resistivity" is used herein to describe the resulting lowered resistivity of the substrate structure

incorporating the resistivity-lowering bodies **26**.

As shown in the illustrated embodiment, a barrier layer **29**, such as may be provided by a thin layer of titanium, for example, may be sputter deposited to line the recess and extend along the backside of the substrate **23** as will be readily appreciated by those skilled in the art. The titanium may have a thickness of about 1000Å, for example. The metal layer **30** includes portions which extend into the recesses and define along with the adjacent portions of the barrier layer **29**, in the illustrated embodiment, the resistivity-lowering bodies **26**.

As would be readily appreciated by those skilled in the art, in other embodiments, the semiconductor device **20** may include only a single device active region. In addition, the semiconductor device **20** in other embodiments may also have only a single resistivity-lowering body **26**.

In the illustrated embodiment, each resistivity-lowering body **26** fills an associated recess of the substrate **23**. By filling the recess, greater mechanical integrity and, thus, greater handling strength may be imparted to the substrate **23**, and, hence, to the overall semiconductor device **20**. Stress reduction may also be provided by filling the recesses. In addition, it may typically be easier from a manufacturing standpoint to completely fill the recesses with a conductive material to form the bodies **26** as will also be readily appreciated by those skilled in the art.

As shown in the bottom plan view of FIG. 2, the semiconductor device **20** prior to the

metallization step to form the contact layer **25** illustratively includes recesses **28** arranged in a grid pattern of intersecting cuts, such as, for example, orthogonal cuts, in the backside of the substrate **23**. The grid pattern may be easily produced by cutting with a conventional saw as used in semiconductor manufacturing as will be appreciated by those skilled in the art. The recesses **28** may be further etched to better prepare the recesses to receive a metallization layer as will also be understood by those skilled in the art. One or more diagonal cuts, not shown, may also be made to increase the total area of the resistivity-lowering bodies **26**.

FIG. 3 illustrates another embodiment of the device **20'** wherein the backside contact layer **25'** is adjacent the barrier layer **29'**, and wherein the contact layer includes portions which partially fill the recesses in the substrate **23'**. In this embodiment the bodies **26'** may further include filling portions of the solder layer **31** as shown in the illustrated embodiment. The solder layer **31** may typically be provided during assembly of the integrated circuit device. In other words, the integrated circuit die is manufactured to include the partially filled recesses and associated bodies **26'** having voids which are filled during final assembly by the illustrated solder layer **31**.

The bottom plan view of FIG. 4 illustrates another embodiment of the semiconductor device **20"** with the recesses **28"** in the form of a series of spaced apart generally cylindrical recesses in the backside of the substrate **23"**. The generally

cylindrical recesses **28"** may be formed by conventional laser etching techniques as will also be readily appreciated by those skilled in the art. The sharp edges produced by the laser etching may be rounded by an additional etching step to better prepare the recesses **28"** to receive the metallization layer which provides the resistivity-lowering bodies **26**, and which may also provide the contact layer **25**. The recesses **28"**, in other embodiments may have shapes other than the illustrated circular cylinders as will be appreciated by those skilled in the art.

Turning now more particularly to FIG. 5, an embodiment of the semiconductor device **40** including a power MOSFET is now described. The device **40** includes a substrate **43**, a backside or drain contact layer **45**, and an active region **42** at the upper surface. A portion of one of the resistivity-lowering bodies **46** is shown in the lower right-hand portion of the cross-sectional view. The body **46** extends into the substrate **43** and is connected to the drain contact layer **45**. The illustrated substrate **43** includes an N+ region **50** adjacent the drain contact layer **45**, and an N- drift region **51** above the N+ region. A source contact layer **53**, and a gate layer **54** and its gate insulating layer **55** are on the upper surface of the substrate **43**. A P region **56** and an N+ region **57** are formed in the substrate adjacent the upper surface of the substrate **43** as illustrated.

Only a single power MOSFET device is illustrated in the semiconductor device **40**, although it will be readily understood by those

skilled in the art that in many applications a plurality of cells of such MOSFET device structures may be formed, such as for a discrete power device. The power MOSFET may also have other equivalent structures as will be readily appreciated by those skilled in the art. In addition, the one or more power MOSFETs may also be included on an integrated circuit with other circuit components as well.

The resistivity-lowering body **46** serves to lower the specific on-resistance of the power MOSFET formed in the substrate **43**. The lowered effective resistivity of the substrate is particularly advantageous for a discrete power MOSFET having a breakdown voltage of less than about 50 V, and, more preferably less than about 30 V. For these devices, the substrate resistivity is a significant overall component of the specific on-resistance of the device.

Another component of the specific on-resistance of the device **40** may be the contact resistance. Accordingly, the substrate may include a more highly doped region, such as the N+ region **50** adjacent the resistivity-lowering bodies **46**, or alternately, a substrate having a lower initial resistivity of about 3 mΩ•cm may be used to reduce the contribution of the contact resistance as will be readily appreciated by those skilled in the art. The more heavily doped substrate region may have a dopant concentration of about 6 X 10^{19} atoms/cm^3, for an N type substrate, for example. The lower initial resistivity substrate may offer an advantage in avoiding an additional doping step as will be appreciated by those skilled in the art.

Turning now more particularly to FIG. 6, a semiconductor device **60** including an insulated gate

bipolar transistor (IGBT) structure is shown also including a portion of a resistivity-lowering body **66** which provides a lower forward voltage drop for the device as will be appreciated by those skilled in the art. The resistivity-lowering body **66** is illustratively formed of doped polysilicon, although metals may also be used. The polysilicon may be doped to about 6×10^{19} atoms/cm^3, for example.

The IGBT illustratively includes a collector contact layer **65**, a P+ layer **70** adjacent the collector contact and formed in the substrate **63**, and an N region **71** of the substrate above the P+ region. An emitter contact **73**, and a gate insulating layer **75** and gate layer **74** are also provided as would be readily understood by those skilled in the art. A P+ region **76** and an N+ region **77** are also formed adjacent the upper surface of the substrate **63**. The semiconductor device **60** may include a plurality of IGBTs, or may include other circuit components as will also be appreciated by those skilled in the art.

Focusing now on the embodiments of the invention including one or more power MOSFETs, the present invention provides a lower specific on-resistance for such devices. In particular, as noted above in the background, wafer thinning is an approach to reduce the substrate electrical and thermal resistance. Unfortunately, wafer thinning is relatively difficult and the resulting thinned wafer may be too fragile to handle for further processing. Wafer yield may also be significantly lowered for thinned wafers.

The present invention provides for a lowered

effective substrate resistivity without requiring thinning, although the invention may also be advantageously used in conjunction with wafer thinning and/or in conjunction with a lower resistivity substrate. The resistivity-lowering bodies may preferably be an electrical conductor having a resistivity less than about 10^{-4} Ω•cm. For example, the material of the bodies may be a metal, such as copper, aluminum or silver which have resistivities approaching 10^{-6} Ω•cm. Typical resistivities for commercially available substrates may be about 2 to 5 mΩ•cm, for example. The resistivity-lowering bodies will, of course, have a resistivity less than the semiconductor material of the substrate, and, for the case of metals such as aluminum, copper and silver, the resistivities are several orders of magnitude lower than for the silicon substrates. Accordingly, as will be seen below, only a relatively small amount of the resistivity-lowering material will be needed to make significant improvements in the specific on-resistance.

The specific on-resistance of the substrate $R_{sp(substrate)}$ including the resistivity-lowering bodies in accordance with the present invention is given to a first order by:

$$R_{sp(substrate)} = \frac{\rho_{si}\,\rho_{body}\,t_{body}}{\lambda\rho_{si} + (1-\lambda)\,\rho_{body}} + \rho_{si}\,(t_{substrate} - t_{body})$$

wherein ρ_{si} and ρ_{body} are the resistivities of the silicon substrate and body material, respectively;

$t_{substrate}$ and t_{body} are the thickneses of the

substrate and bodies, respectively; and

λ is a ratio of the area of the bodies to the total substrate area.

A set of examples where the body material is aluminum, and the substrate has a thickness of 14 mil and a resistivity of 4.5 mΩ•cm are plotted in FIG. 7. More particularly, the uppermost horizontal plot with the diamond markers illustrates the specific on-resistance of the substrate without any resistance-lowering bodies. The plot second from the top and having the square markers is for a thickness of the aluminum bodies of 4 mil. The plot third from the top and having the triangular markers is for a thickness of the bodies of 6 mil. Lastly, the bottom plot indicated with X markers is for a thickness of the bodies of 8 mil. The X-axis is the ratio or proportion of the area of the bodies to the die area.

The term area is correct when the bodies have a uniform shape extending into the substrate. In other words, the analysis assumes that the sidewalls of the recesses and bodies are at 90° from the backside surface so that the area of the bodies is the same along their depth of penetration into the substrate. However, the area may also be an effective or average area as will be readily appreciated by those skilled in the art to cover other shapes of recesses and bodies. For example, the area for trapezoidal shape recesses and bodies is larger at the backside surface than at the termination in the substrate. Accordingly, in this instance the term area will be understood to define the effective area defined by the trapezoidal bodies.

The plotted results indicate, for example, that for a body thickness of 8 mil, the aluminum

bodies need only cover about one percent of the area to lower the specific on-resistance to less than half its original value (160 lowered to about 70 $\mu\Omega \cdot cm^2$). The marginal lowering of the specific on-resistance levels off beyond about 1 percent, for all three of the body thicknesses plotted in FIG. 7. In addition, a substantial marginal lowering of resistivity occurs for a proportion of as little as 0.4 percent as also seen from the plots of FIG. 7. Accordingly, the recesses and associated resistivity-lowering bodies preferably define a proportion of the semiconductor substrate area adjacent the device active region greater than or equal to about 0.4 percent. As noted, marginal gains for a proportional area above 1 percent are slight. Thus, a preferred range may be between about 0.4 and 1 percent, for example, when using a conductive metal, such as aluminum, for the material of the bodies.

The recesses and associated resistivity-lowering bodies provide a significant lowering of the specific on-resistance with a body thickness of only 4 mils for a 14 mil substrate. Accordingly, the thickness of the resistivity-lowering bodies may be greater than or equal to about 25 percent of the thickness of the substrate.

The semiconductor substrate may comprise silicon, for example. In addition, since a metal, such as copper or aluminum may be used for the resistivity-lowering bodies, the thermal conductivity of these materials is typically higher than silicon, for example. Accordingly, power dissipation from the substrate is also enhanced by the presence of the resistivity-lowering bodies. The plots of FIG. 8 illustrate the specific thermal resistances for the substrate for each of the four

thickness of bodies as explained above with reference to FIG. 7. In particular, these plots indicate that the specific thermal resistance is not significantly lowered until the percentage of the area of the bodies is increased beyond 1 percent, and more preferably, beyond 10 percent or more.

Turning now to FIGS. 9 and 10 plots of specific on-resistance and specific thermal resistance, respectively, are given for a second set of examples where copper is used as the material for the resistivity-lowering bodies. In particular, the substrate has a thickness of 14 mil and a resistivity of 4.5 mΩ•cm. The uppermost plot with the diamond markers illustrates the specific on-resistance of the substrate without any resistance-lowering bodies. The plot having the square markers is for a thickness of the copper bodies of 4 mil. The plot third from the top and having the triangular markers is for a thickness of the bodies of 6 mil. The bottom plot indicated with X markers is for a thickness of the bodies of 8 mil. Because of the slightly lower electrical resistivity of copper as compared to aluminum, the lowering of the specific on-resistance of the substrate is greater for this set of examples using copper. Because copper also has a lower thermal resistivity, it also provides a slight improvement as compared to aluminum.

Turning now to FIGS. 11 and 12, similar plots of specific on-resistance and specific thermal resistance are shown for a third set of examples where the material of the bodies is silver. Silver has a lower electrical resistivity than both copper and aluminum and this is reflected in the slightly better performance in lowering the specific on-

resistance. The various plots are for the same conditions/parameters as described above, but for the use of silver as the material for the resistivity-lowering bodies. Accordingly, these plots need no further discussion herein.

The use of the resistivity-lowering bodies is also advantageous even for a substrate having a relatively low initial resistivity as will understood with reference to the plots of FIG. 13. In particular, in this set of examples the substrate has a thickness of 14 mil and a resistivity of only 2.6 mΩ•cm. Aluminum is the material used for the bodies in this example set. The uppermost horizontal plot with the diamond markers illustrates the specific on-resistance of the substrate without any resistivity-lowering bodies. The plot having the square markers is for a thickness of the bodies of 4 mil. The plot third from the top and having the triangular markers is for a thickness of the bodies of 6 mil. The bottom plot indicated with X markers is for a thickness of the bodies of 8 mil. This additional set of examples indicates the desirability of the resistivity-lowering bodies even for a substrate having a relatively low initial resistivity.

FIG. 14 provides yet another set of examples wherein the starting substrate is thinner than for the example sets given above. More particularly, the substrate for these illustrated examples is only 10 mil thick. Aluminum is used for the material of the bodies. Each of the plots is for the respective thicknesses as described above. Since the percentage of penetration of the bodies with respect to the overall thickness of the substrate is higher for the 10 mil substrate, the lowering of the specific on-resistance is also

greater.

A method aspect of the invention is for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity. The method preferably comprises the steps of: forming at least one device active region in the semiconductor substrate adjacent a first surface thereof; forming at least one recess extending from a second surface of the substrate, opposite the first surface, into interior portions of the semiconductor substrate; and forming at least one resistivity-lowering body in the least one recess of the semiconductor substrate. The at least one resistivity-lowering body preferably comprises a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate. The method also preferably includes the step of forming an electrical contact layer on the second surface of the semiconductor substrate being electrically connected to the at least one resistivity-lowering body.

As described above with respect to the embodiment of the semiconductor device 20 in FIG. 2, a semiconductor saw may be used to form a pattern of recesses 28 by cutting into the backside of the wafer before the individual die are cut from the wafer. A recess 28 in the form of a trench may have relatively sharp corners or edges. Accordingly, a further etching step may be performed to soften the corners and round the edges to better receive a metallization layer. A trapezoidal shape may also be desired for receiving a polysilicon deposition. Chemo-mechanical polishing (CMP) techniques may also be used as will be readily understood by those skilled in the art.

The pattern of recesses and associate bodies may define a grid having a spacing of about 200-2000 μm, and wherein the width of each body is about 10-100 μm, for example.

Of course those of skill in the art will appreciate other equivalent methods for forming the recesses and filling same with the resistivity-lowering bodies. In addition, other devices, such as MOS-controlled thyristors (MCTs), for example, and other similar devices may also benefit from the substrate resistivity lowering concepts of the present invention as will be appreciated by those skilled in the art. A microprocessor integrated circuit having a general schematic cross-section as shown in FIG. 1 may also benefit especially from the increased thermal conductivity of the bodies to thereby dissipate heat. Accordingly, many modifications and other embodiments of the invention will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is to be understood that the invention is not to be limited to the specific embodiments disclosed, and that modifications and embodiments are intended to be included within the scope of the appended claims.

THAT WHICH IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate having opposing first and second surfaces, and having at least one recess extending from the second surface into interior portions;

at least one device active region formed in said semiconductor substrate adjacent the first surface thereof;

an electrical contact layer on the second surface of said semiconductor substrate; and

at least one resistivity-lowering body positioned in said at least one recess of said semiconductor substrate and connected to said electrical contact layer, said at least one resistivity-lowering body comprising a material having an electrical resistivity lower than an electrical resistivity of said semiconductor substrate to thereby lower an effective electrical resistivity thereof.

2. A semiconductor device according to Claim 1 wherein said at least one resistivity-lowering body fills an associated recess.

3. A semiconductor device according to Claim 1 further comprising a barrier layer positioned between said at least one resistivity-lowering body and the corresponding recess.

4. A semiconductor device according to Claim 1 wherein said at least one resistivity-lowering body comprises an electrical conductor having a resistivity less than about 10^{-4} Ω•cm.

5. A semiconductor device according to Claim 1 wherein said at least one recess and associated resistivity-lowering body defines a proportion of the semiconductor substrate area adjacent said at least one device active region greater than about 0.4 percent.

6. A semiconductor device according to Claim 1 wherein said at least one recess and associated resistivity-lowering body extends into said semiconductor substrate a distance greater than about 25 percent of a thickness of said semiconductor substrate.

7. A semiconductor device according to Claim 1 wherein said at least one recess and associated resistivity-lowering body comprises an array of recesses and associated resistivity-lowering bodies.

8. A semiconductor device according to Claim 7 wherein said array of recesses and associated resistivity-lowering bodies are arranged in a grid pattern.

9. A semiconductor device according to Claim 1 wherein said at least one device active region comprises at least one active region of a metal-oxide semiconductor field-effect transistor (MOSFET).

10. A semiconductor device according to Claim 9 wherein said MOSFET has a breakdown voltage of less than about 50 volts.

11. A semiconductor device according to Claim

1 wherein said at least one device active region comprises at least one active region of an insulated gate bipolar transistor (IGBT).

12. A semiconductor device according to Claim 1 wherein said at least one device active region comprises at least one active region of a microprocessor.

13. A semiconductor device according to Claim 1 wherein said substrate further comprises a relatively highly doped layer adjacent said at least one resistivity-lowering body.

14. A semiconductor device according to Claim 1 wherein said semiconductor substrate comprises silicon.

15. A semiconductor device according to Claim 14 wherein the silicon substrate has an electrical resistivity of less than about 3 mΩ•cm.

16. A semiconductor device according to Claim 1 wherein said at least one resistivity-lowering body has a thermal resistivity lower than a thermal resistivity of said semiconductor substrate.

17. A semiconductor device according to Claim 1 wherein said at least one resistivity-lowering body comprises at least one of copper, silver, aluminum, and solder.

18. A semiconductor device according to Claim 1 wherein said at least one resistivity-lowering body comprises polysilicon.

19. A semiconductor device comprising:

a semiconductor substrate having opposing first and second surfaces, and having at least one recess extending from the second surface into interior portions;

at least one metal-oxide semiconductor field-effect transistor (MOSFET) active region formed in said semiconductor substrate adjacent the first surface thereof;

a conduction terminal contact on the second surface of said semiconductor substrate; and

at least one resistivity-lowering body positioned in said at least one recess of said semiconductor substrate and connected to said conduction terminal contact, said at least one resistivity-lowering body comprising a material having an electrical resistivity lower than an electrical resistivity of said semiconductor substrate.

20. A semiconductor device according to Claim 19 wherein said at least one resistivity-lowering body fills an associated recess.

21. A semiconductor device according to Claim 19 further comprising a barrier layer positioned between said at least one resistivity-lowering body and the corresponding recess.

22. A semiconductor device according to Claim 19 wherein said at least one resistivity-lowering body comprises an electrical conductor having a resistivity less than about 10^{-4} Ω•cm.

23. A semiconductor device according to Claim 19 wherein said at least one recess and associated

resistivity-lowering body defines a proportion of the semiconductor substrate area adjacent said at least one MOSFET active region greater than about 0.4 percent.

24. A semiconductor device according to Claim 19 wherein said at least one recess and associated resistivity-lowering body extends into said semiconductor substrate a distance greater than about 25 percent of a thickness of said semiconductor substrate.

25. A semiconductor device according to Claim 19 wherein said at least one recess and associated resistivity-lowering body comprises an array of recesses and associated resistivity-lowering bodies.

26. A semiconductor device comprising:

a semiconductor substrate having opposing first and second surfaces;

at least one device active region formed in said semiconductor substrate adjacent the first surface thereof;

an electrical contact layer on the second surface of said semiconductor substrate; and

at least one resistivity-lowering body connected to said electrical contact layer and extending into interior portions of said semiconductor substrate, said at least one resistivity-lowering body comprising a material having an electrical resistivity lower than about 10^{-4} Ω•cm;

said at least one recess and associated resistivity-lowering body defining a proportion of the semiconductor substrate area adjacent said at

least one device active region greater than about 0.4 percent and extending into said semiconductor substrate a distance greater than about 25 percent of a thickness of said semiconductor substrate.

27. A semiconductor device according to Claim 26 further comprising a barrier layer positioned between said at least one resistivity-lowering body and the corresponding recess.

28. A semiconductor device according to Claim 26 wherein said at least one recess and associated resistivity-lowering body comprises an array of recesses and associated resistivity-lowering bodies.

29. A semiconductor device according to Claim 26 wherein said at least one device active region comprises at least one active region of a metal-oxide semiconductor field-effect transistor (MOSFET).

30. A semiconductor device according to Claim 26 wherein said at least one device active region comprises at least one active region of an insulated gate bipolar transistor (IGBT).

31. A semiconductor device according to Claim 26 wherein said at least one device active region comprises at least one active region of a microprocessor.

32. A semiconductor device comprising:

a semiconductor substrate having opposing first and second surfaces;

at least one device active region formed in

said semiconductor substrate adjacent the first surface thereof;

an electrical contact layer on the second surface of said semiconductor substrate; and

at least one body electrically conductive metal connected to said electrical contact layer and extending into interior portions of said semiconductor substrate, said at least one electrically conductive metal body comprising a material having an electrical resistivity lower than an electrical resistivity of said semiconductor substrate.

33. A semiconductor device according to Claim 32 wherein said at least one electrically conductive metal body comprises at least one of aluminum, copper, silver, and solder.

34. A semiconductor device according to Claim 32 wherein said at least one recess and associated electrically conductive metal body defines a proportion of the semiconductor substrate area adjacent said at least one device active region greater than about 0.4 percent.

35. A semiconductor device according to Claim 32 wherein said at least one recess and associated electrically conductive metal body extends into said semiconductor substrate a predetermined proportion of a thickness of said semiconductor substrate greater than about 25 percent.

36. A semiconductor device according to Claim 32 wherein said at least one recess and associated electrically conductive metal body comprises an array of recesses and associated bodies.

37. A semiconductor device according to Claim 32 wherein said at least one device active region comprises at least one active region of a metal-oxide semiconductor field-effect transistor (MOSFET).

38. A semiconductor device according to Claim 32 wherein said at least one device active region comprises at least one active region of an insulated gate bipolar transistor (IGBT).

39. A semiconductor device according to Claim 32 wherein said at least one device active region comprises at least one active region of a microprocessor.

40. A method for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method comprising the steps of:

forming at least one device active region in the semiconductor substrate adjacent a first surface thereof;

forming at least one recess extending from a second surface of the substrate, opposite the first surface, into interior portions of the semiconductor substrate;

forming at least one resistivity-lowering body in the least one recess of the semiconductor substrate, the at least one resistivity-lowering body comprising a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate; and

forming an electrical contact layer on the second surface of the semiconductor substrate being electrically connected to the at least one

resistivity-lowering body.

41. A method according to Claim 40 wherein the step of forming the at least one resistivity-lowering body comprises filling an associated recess.

42. A method according to Claim 40 further comprising the step of forming a barrier layer lining the at least one recess.

43. A method according to Claim 40 wherein the step of forming the at least one resistivity-lowering body comprises forming same using an electrical conductor having an electrical resistivity less than about 10^{-4} Ω•cm.

44. A method according to Claim 40 wherein the steps of forming the at least one recess and associated resistivity-lowering body comprises forming same to define a proportion of the semiconductor substrate area adjacent the at least one device active region greater than about 0.4 percent.

45. A method according to Claim 40 wherein the steps of forming the at least one recess and associated resistivity-lowering body comprises forming same to extend into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

46. A method according to Claim 40 wherein the step of forming the at least one recess and associated resistivity-lowering body comprises forming an array of recesses and associated

resistivity-lowering bodies.

47. A method according to Claim 40 wherein the step of forming the array of recesses and associated resistivity-lowering bodies comprises forming same to be arranged in a grid pattern.

48. A method according to Claim 47 wherein the step of forming the grid pattern comprises cutting trenches in the second surface of said semiconductor substrate.

49. A method according to Claim 40 wherein the step of forming the at least one device active region comprises forming at least one device active region for a metal-oxide semiconductor field-effect transistor (MOSFET).

50. A method according to Claim 40 wherein the step of forming the at least one device active region comprises forming at least one device active region for an insulated gate bipolar transistor (IGBT).

51. A method according to Claim 40 wherein the step of forming the at least one device active region comprises forming at least one active region of a microprocessor.

SEMICONDUCTOR DEVICE HAVING REDUCED EFFECTIVE SUBSTRATE RESISTIVITY AND ASSOCIATED METHODS

Abstract of the Disclosure

A semiconductor device includes at least one device active region formed in a first surface of a semiconductor substrate, an electrical contact layer on a second surface of the semiconductor substrate, and at least one resistivity-lowering body positioned in a corresponding recess in the substrate and connected to the electrical contact layer. The body preferably comprises a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate to thereby lower an effective electrical resistivity of the substrate. The device active region may be an active region of a power control device, such as a MOSFET or IGBT, for example. The body may preferably comprise an electrical conductor such as copper, aluminum, silver, solder, or doped polysilicon. The at least one recess and associated resistivity-lowering body preferably defines a proportion of the semiconductor substrate area adjacent the device active region greater than about 0.4 percent, and may extend into the semiconductor substrate a distance greater than about 25 percent of a thickness of the substrate.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
ZENG

Serial No. **Not yet assigned**

Filing Date: **Herewith**

For: **SEMICONDUCTOR DEVICE HAVING REDUCED EFFECTIVE SUBSTRATE RESISTIVITY AND ASSOCIATED METHODS**

) Examiner: A. Wilson
)
) Art Unit: 2815

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Eric Link
(TYPED OR PRINTED NAME OF PERSON MAILING PAPER OR FEE)

[signature]
(SIGNATURE OF PERSON MAILING PAPER OR FEE)

TRANSMITTAL OF FORMAL DRAWINGS

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed are seven (7) sheets of formal drawings to be filed in the above-identified patent application.

Respectfully submitted,

[signature]

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Attorney for Applicant

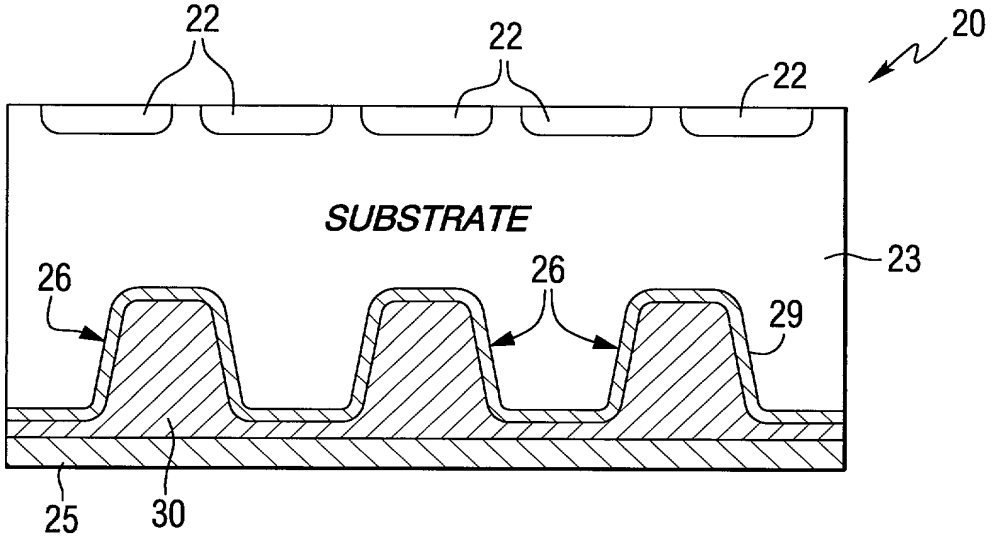


FIG. 1

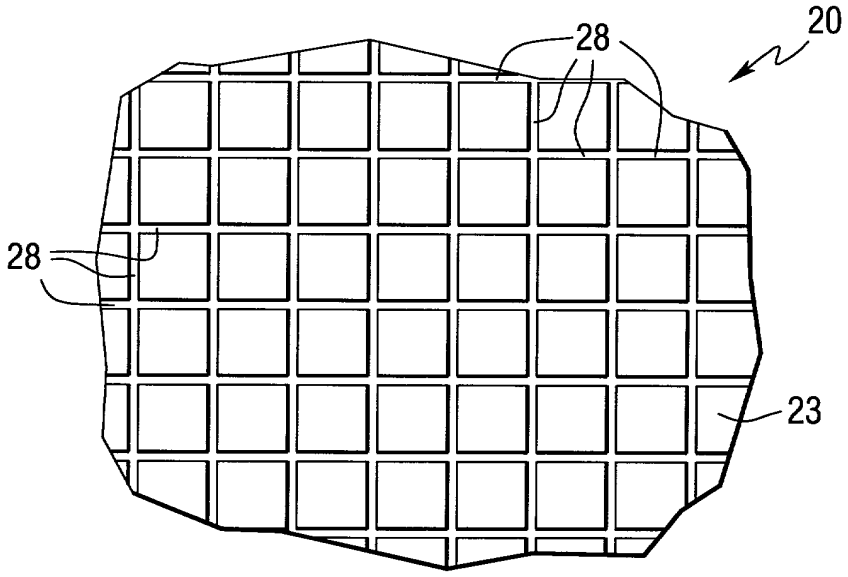


FIG. 2

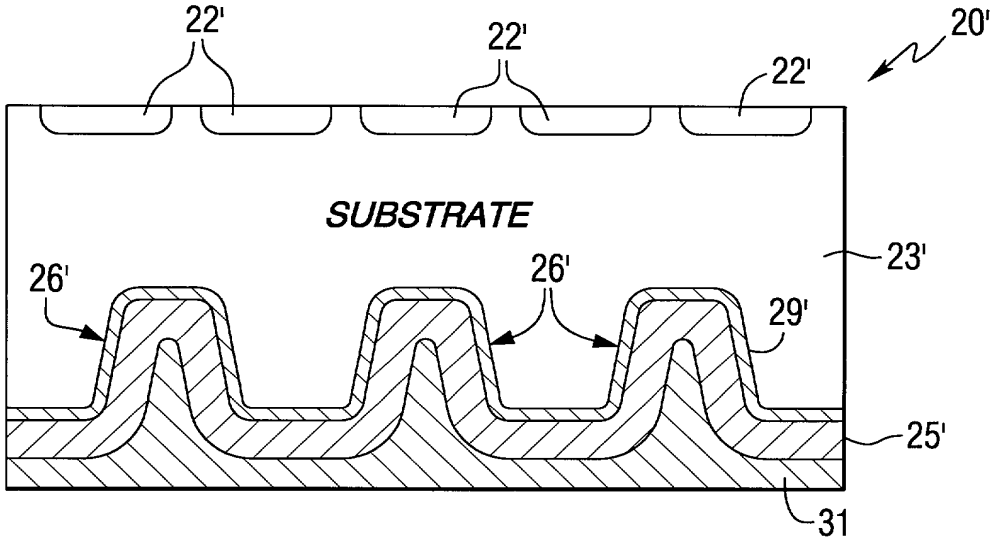


FIG. 3

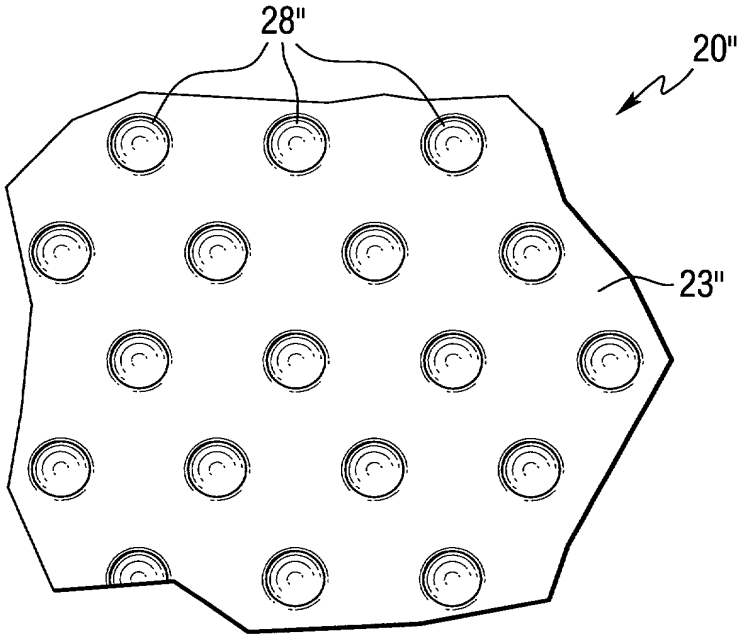
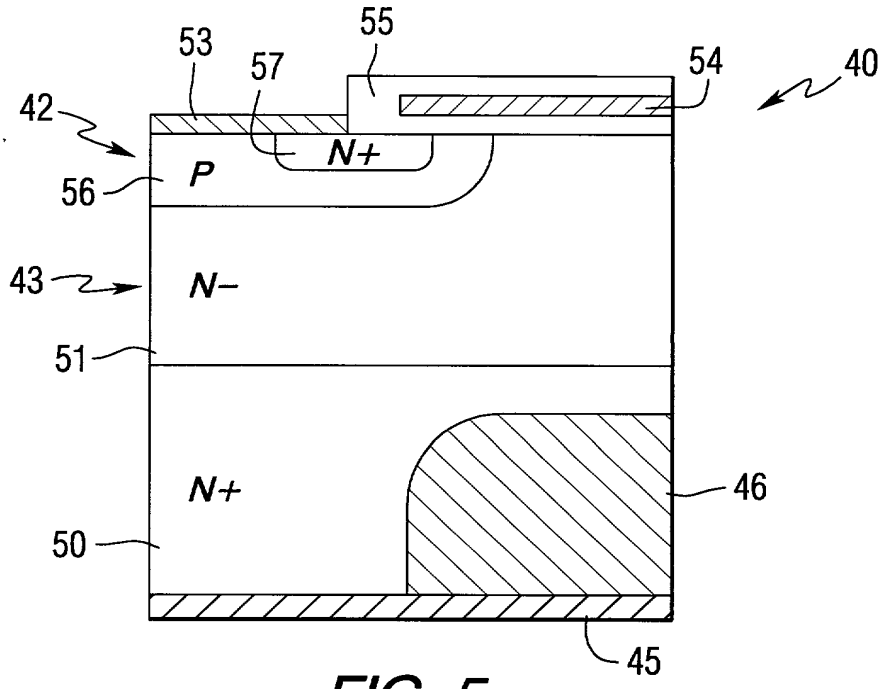


FIG. 4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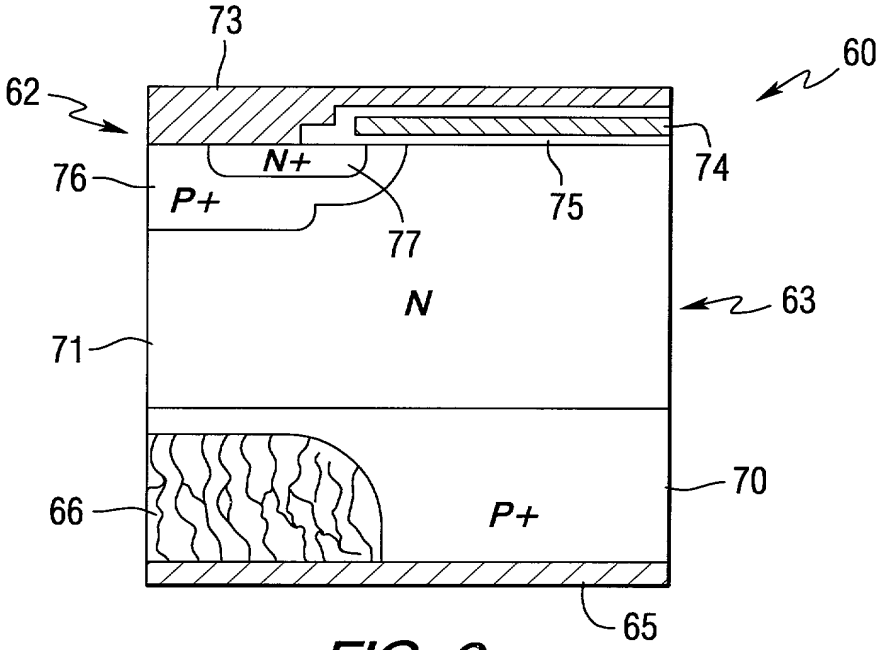
57
54
40
42
N+
P
56
43
N–
51
N+
46
50
45

FIG. 5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71
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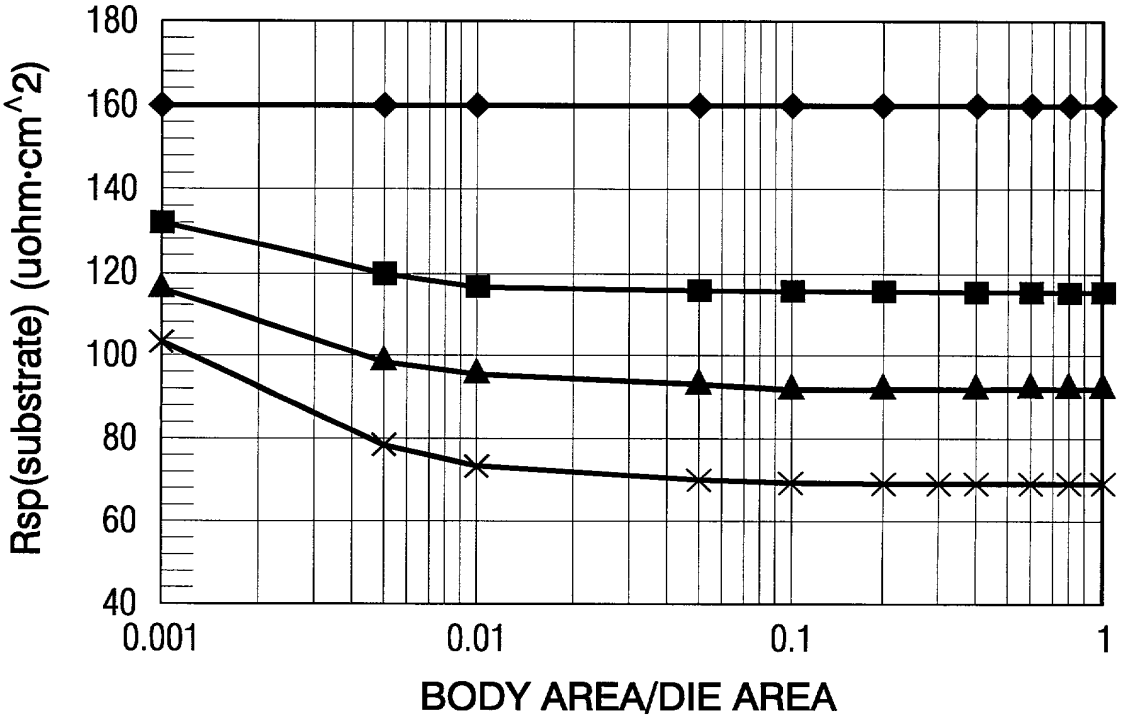
66
P+
65

FIG. 6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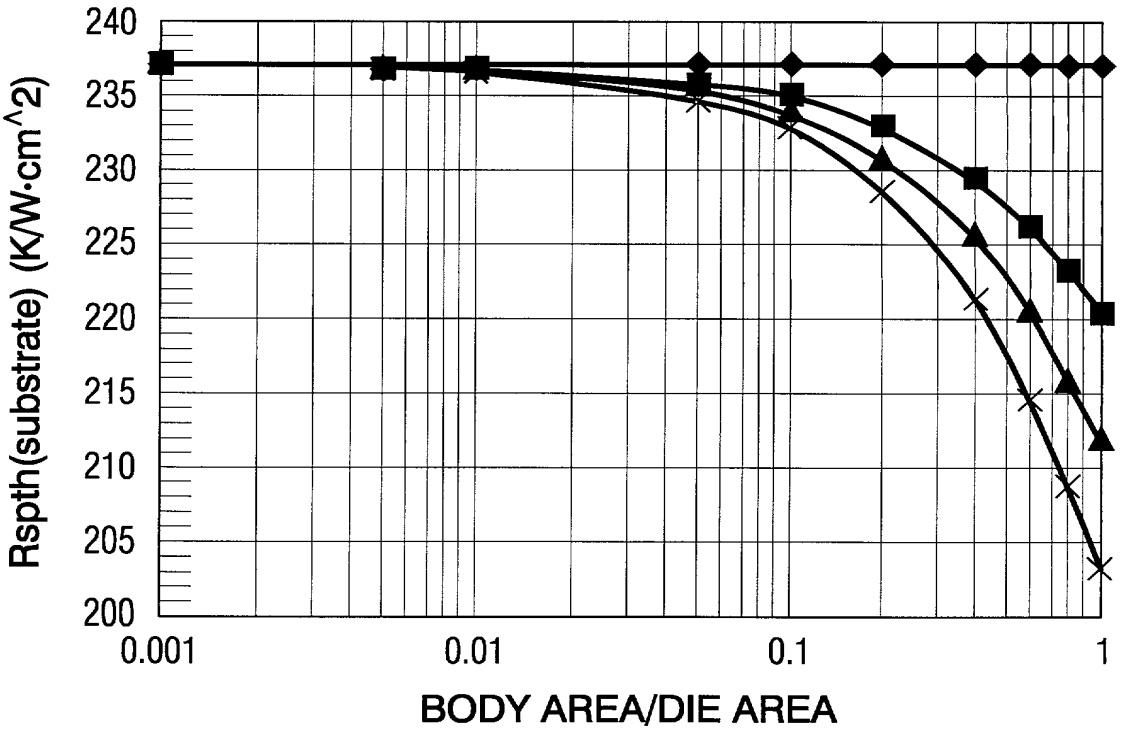
160
140
120
100
80
60
40
Rsp(substrate) (uohm·cm^2)
0.001
0.01
0.1
1
BODY AREA/DIE AREA

FIG. 7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230
225
220
215
210
205
200
Rspth(substrate) (K/W·cm^2)
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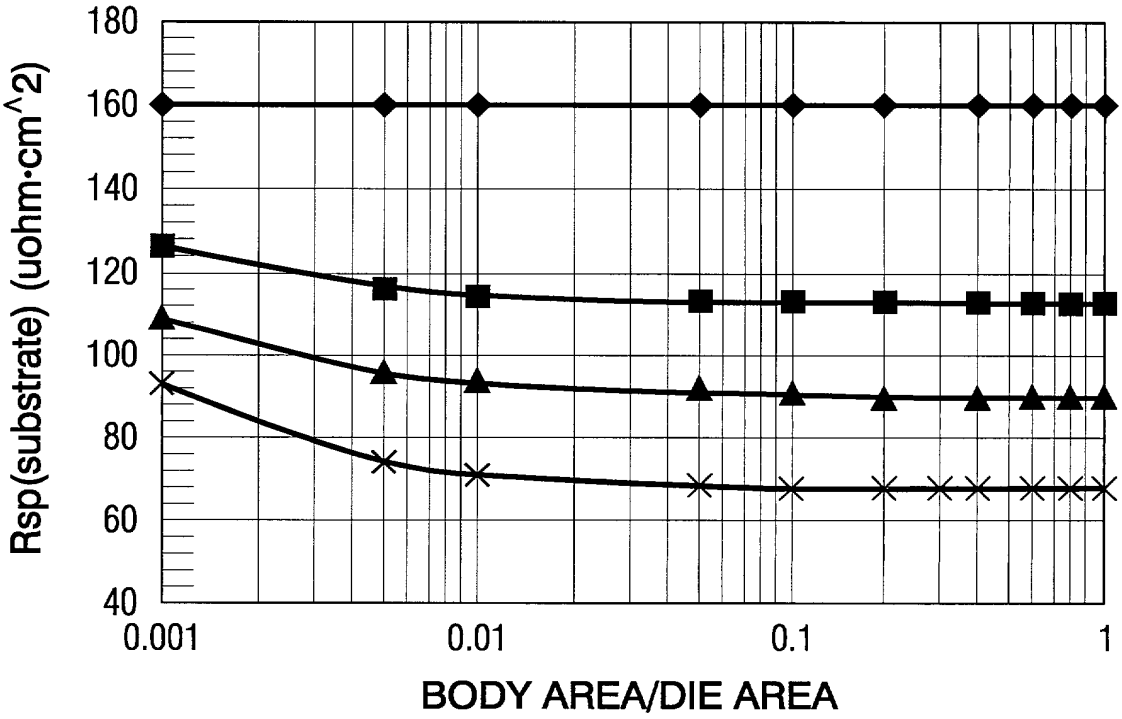
0.01
0.1
1
BODY AREA/DIE AREA

FIG. 8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140
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Rsp(substrate) (uohm·cm^2)
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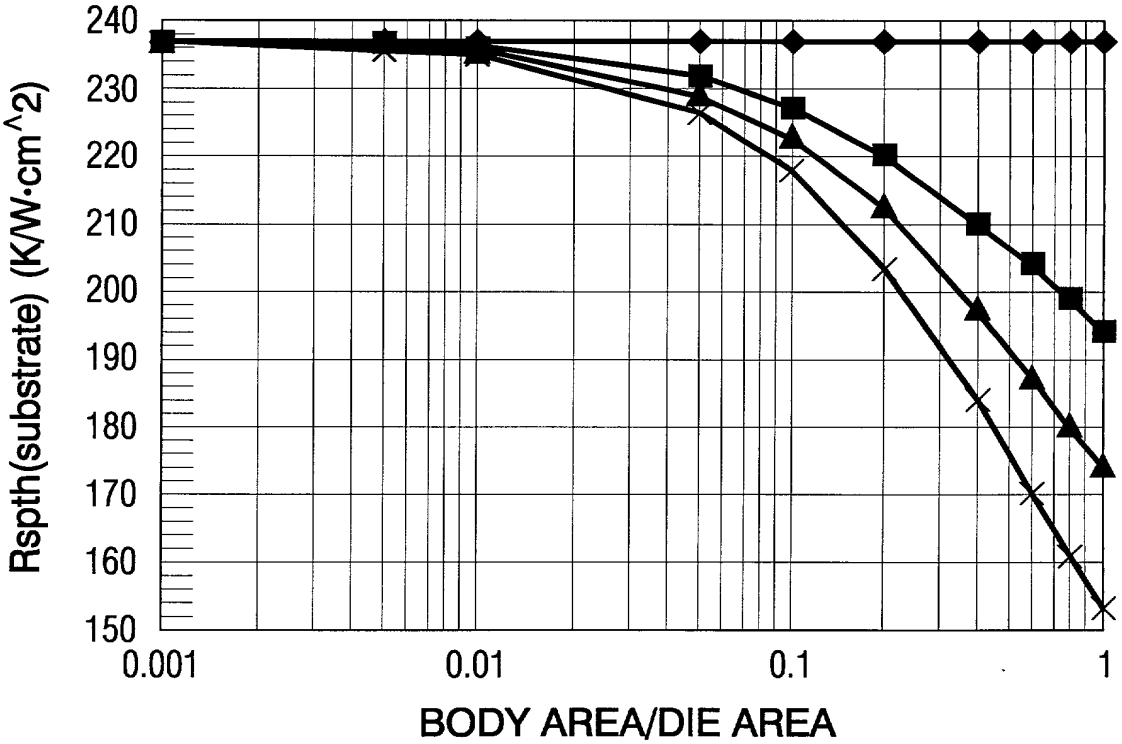
0.01
0.1
1
BODY AREA/DIE AREA

FIG. 9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200
190
180
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160
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Rspth(substrate) (K/W·cm^2)
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0.01
0.1
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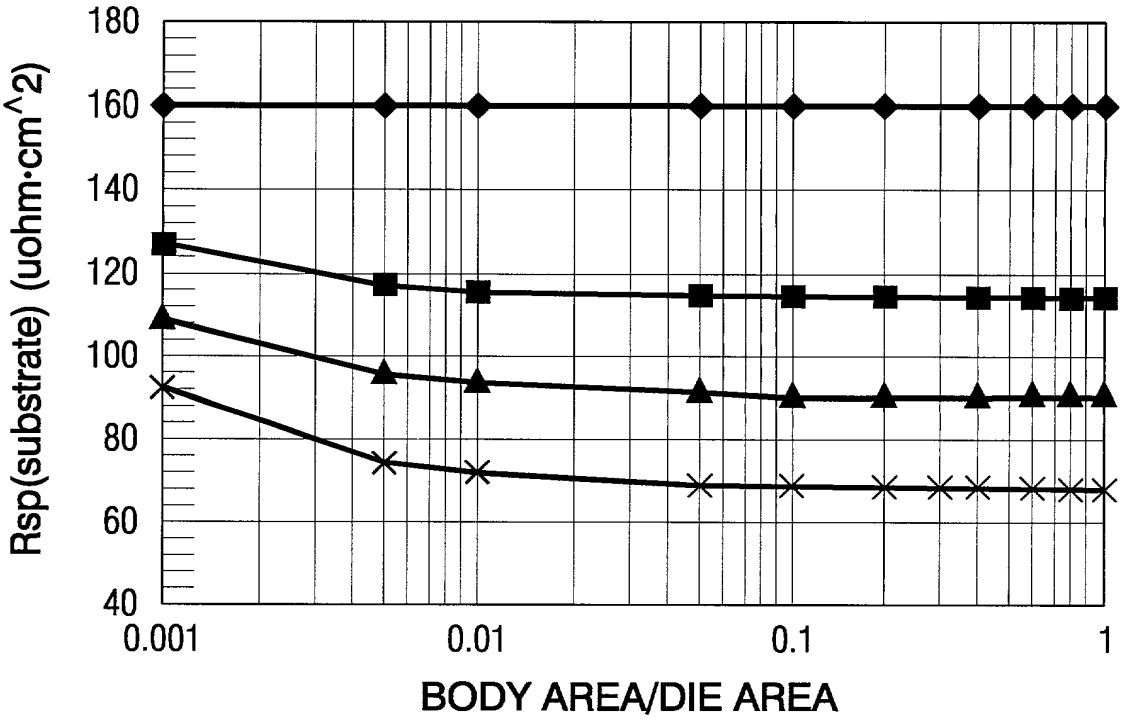
BODY AREA/DIE AREA

FIG. 10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160
140
120
100
80
60
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Rsp(substrate) (uohm·cm^2)
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0.01
0.1
1
BODY AREA/DIE AREA

FIG. 11

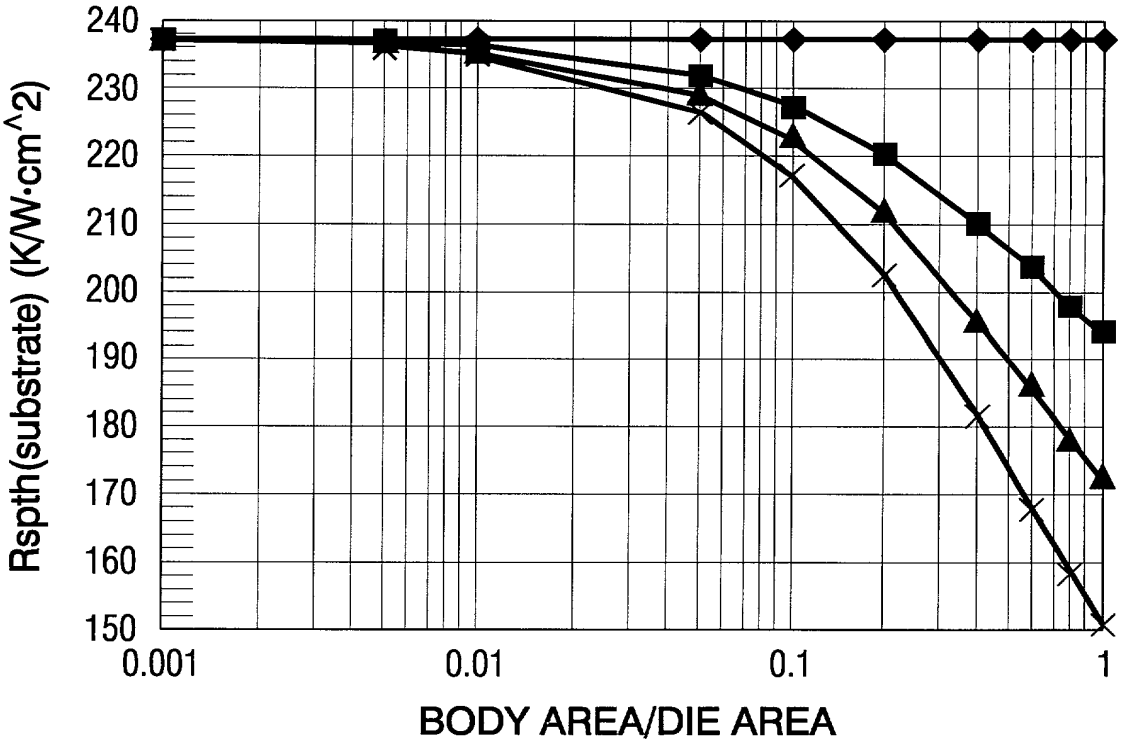
240
230
220
210
200
190
180
170
160
150
Rspth(substrate) (K/W·cm^2)
0.001
0.01
0.1
1
BODY AREA/DIE AREA

FIG. 12

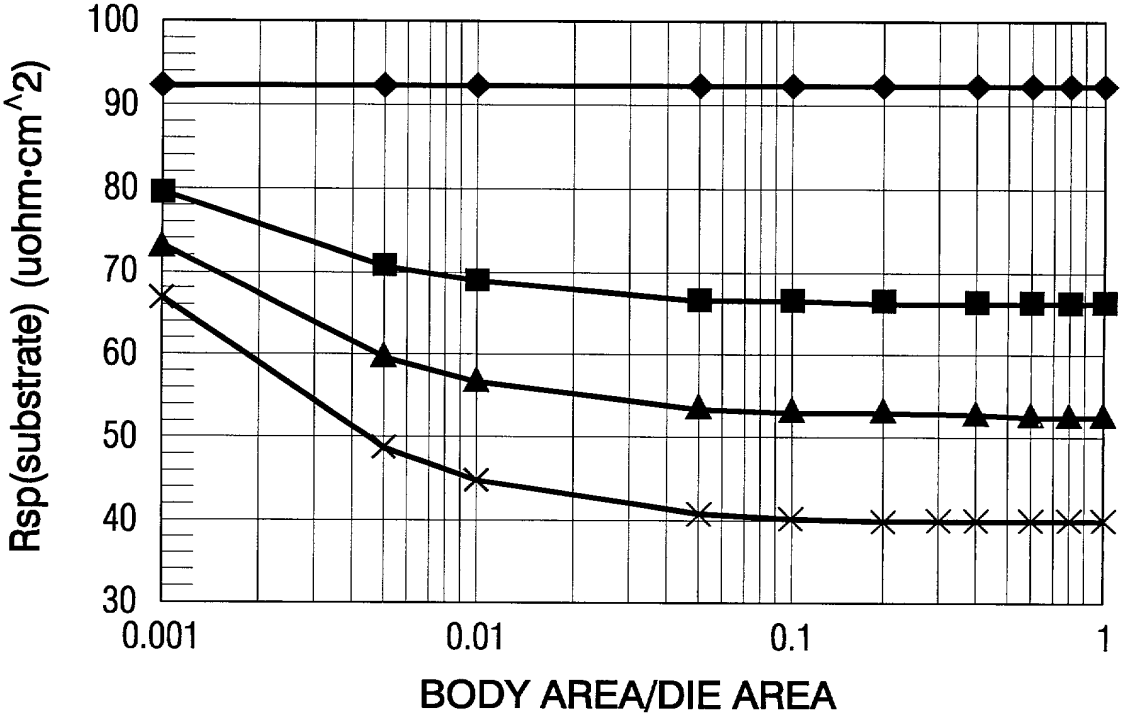
100
90
80
70
60
50
40
30
Rsp(substrate) (uohm·cm^2)
0.001
0.01
0.1
1
BODY AREA/DIE AREA

FIG. 13

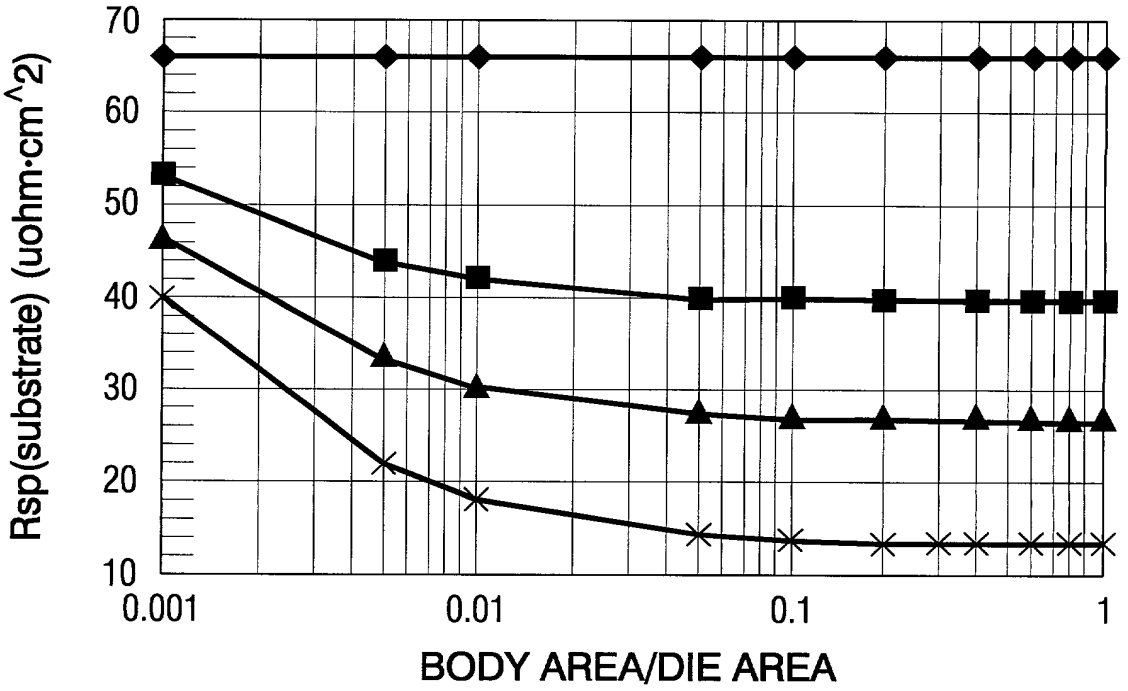
70
60
50
40
30
20
10
Rsp(substrate) (uohm·cm^2)
0.001
0.01
0.1
1
BODY AREA/DIE AREA

FIG. 14

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney Docket No.: **SE-1433-PD (50021)**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **SEMICONDUCTOR DEVICE HAVING REDUCED EFFECTIVE SUBSTRATE RESISTIVITY AND ASSOCIATED METHODS**, the specification of which:

(check one)

_____ is attached hereto

__X__ was filed on ___June 30, 1998___

as Application Serial No. 09/107,721

and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulation, 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the of the application on which priority is claimed:

Prior Foreign Application(s) Priority Claimed

(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No

I hereby claim the benefit under Title 35, United States Code, 120, of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Appln Serial No.)	(Filing Date)	(Status) (patented, pending, aban.)
(Appln Serial No.)	(Filing Date)	(Status) (patented, pending, aban.)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

English Language Declaration

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorneys to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: **Christopher F. Regan**, Reg. No. 34,906; **Herbert L. Allen**, Reg. No. 25,322; **David L. Sigalow**, Reg. No. 36,006; **Jeffrey S. Whittle**, Reg. No. 36,382; **Richard K. Warther**, Reg. No. 32,180; **Michael W. Taylor**, Reg. No. 43,182; **Henry Estevez**, Reg. No. 37,823; **Carl M. Napolitano**, Reg. No. 37,405; **Jacqueline E. Hartt**, Reg. No. 37,845; **Leslie J. Hart**, Reg. No. 26,462; **Harry M. Fleck**, Reg. No. 24,704; **John L. DeAngelis**, Reg. No. 30,622; **Ferdinand Romano**, Reg. No. 32,752; **Joel I. Rosenblatt**, Reg. No. 26,025; **Daniel J. Staudt**, 34,733; **Frederick R. Jorgenson**, 38,196; **Dennis L. Cook**, Reg. No. 30,826; and **Bidyut K. Niyogi**, Reg. No. 27,071.

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